REMARKS/ARGUMENTS

The final Office Action dated April 7, 2006 has been carefully considered. Claims 1 and 4-11 are pending in the present application with claims 1 and 11 in independent form.

Claims 1, 4, 5, 8 and 11 have been rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 6,456,170 to Segawa et al. in view of either Japanese Patent Publication No. JP01157612 to Daisuke and either U.S. Patent Publication No. 2004/0164777 to Yasuda or U.S. Patent No. 4,734,650 to Alley et al.

The Examiner contends that figures 11 and 22 and the relevant text related thereto of Segawa et al. disclose substantially all of the features of claim 1. The Examiner concedes that Segawa is silent as to the construction of the variable current source and silent as to the variable current sources including a switching element wherein a digital to analog converter is provided to provide the analog signal for the switching element. However, the Examiner contends that Daisuke discloses a variable current source with a passive element for setting the minimum current. Further, the Examiner contends that digital control is well known for setting an analog value in a voltage controlled oscillator (VCO) and contends that both Yasuda and Alley et al. disclose this feature.

By this Amendment, Applicant has amended claim 1 to claim an adjustable oscillator circuit for producing a pulsed output, comprising a timing capacitor; an adjustable current source coupled to the capacitor for charging the capacitor at an adjustable rate; a threshold circuit comprising a comparator for changing a charging or discharging state of the capacitor based on a charge value of the capacitor; the threshold circuit including a first threshold value circuit providing a first threshold value to the comparator for comparison with the charge value of the capacitor when the capacitor is in a charging state and a second threshold value circuit providing a second threshold value to the comparator for comparison with the charge value of the capacitor when the capacitor is in a discharging state, further comprising a first gating switch coupled between a comparator input and the first threshold value circuit and a second gating switch coupled between the comparator input and the second threshold value circuit, said first and second gating switches responsive to an output of the comparator to determine which of the first

and second threshold values is provided to the comparator input; a first switch in the adjustable current source operable to vary the current supplied to the capacitor for charging the capacitor at the adjustable rate; a digital to analog converter coupled to a control input of the first switch and operable to receive input digital data and to provide an analog control input of the first control signal to the switch to vary the current supplied to the capacitor based on the input digital data thereby to charge the capacitor at the adjustable rate determined by the input digital data; further comprising a second switch coupled to said capacitor for discharging said capacitor and having a control input coupled to the comparator output, said first gating switch providing said first threshold value to the comparator and allowing said capacitor to be charged until the charge value of said capacitor substantially equals said first threshold value, said second gating switch providing said second threshold value to the comparator while said second switch discharges said capacitor and allowing said capacitor to be discharged until said capacitor charge value is substantially equal to said second threshold value.

The art cited by the Examiner fails to teach or suggest the claimed combination including a threshold circuit with the claimed first and second threshold value circuits, the first and second gating circuits, and the first and second switches, which set, respectively, the adjustable charging rate and the discharging rate, together with a digital control for setting the charging rate via the D/A converter. While the Examiner has cited various prior art references which show various aspects of oscillator control circuitry, it is submitted that the claimed combination which includes both digital and analog control, is not obvious in view of the disparate references cited.

Claims 5-9 and 11 have been canceled. The remaining claims depend from claim 1 and are submitted therefore also to be in condition for allowance.

A good faith effort has been made to place the claims in condition for allowance after the Final Office Action. It is submitted that no new issues have been presented which would require a further search. Accordingly, it is submitted that all claims remaining are in condition for allowance.

Favorable reconsideration of the present application is respectfully requested.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop A.F., Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 7, 2006

Louis C. Dujmich
Name of applicant, assignee or Registered Representative

Signature

July 7, 2006
Date of Signature

LCD/jh

Respectfully submitted,

Louis C. Dujmich
Registration No.: 30,625
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700